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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,220	06/09/2005	Ray Burke	P-0206-PCT-PA	9364

22145 7590 05/30/2007

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EXAMINER	
BAISA, JOSELITO SASIS	
ART UNIT	**PAPER NUMBER**
2832	

MAIL DATE	DELIVERY MODE
05/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,220	BURKE ET AL.	
	Examiner	Art Unit	
	Joselito Baisa	2832	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,12-14,17,18,20,21,28-34,36-39,42-47 and 55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-9,12-14,17,18,20,21,28-34,36-39,42-47 and 55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/9/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-9, 12, 17, 18, 20, 21, 28-34, 36-39, 44-47 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Inagaki et al. [6724638].

Inagaki discloses a first laminar electrode 21,

a second laminar electrode 22,

an element of electronically active material 23 sandwiched between first laminar electrode 21 and second laminar electrode 22,

a region of insulating material (30a, 30c, 38a, 38b, 40) enclosing first laminar electrode 21, second laminar electrode 22 and element of active material 23, wherein the region of insulating material comprises a first layer (30a, 30c, 38a, 38b, 40) of insulating material covering the first laminar electrode and a second layer (30a, 30c, 38a, 38b, 40) of insulating material covering the second laminar electrode 22 [Col. 17, Lines 33-39, Figure 7],

a first terminal 58 for facilitating an external electrical connection to the first laminar electrode 21,

a second terminal 58 for facilitating an external electrical connection to the second laminar electrode 22,

a first conductive interconnection 60 that passes through the region of first layer (30a, 40) of insulating material to electrically connect the first terminal 58 and the first laminar electrode 21, a second conductive interconnection 60 that passes through the region of second layer (30a, 40) of insulating

material to electrically connect the second terminal 58 and the second laminar electrode 22 [Col. 18, Lines 11-25, Figure 7], and

further comprising a third terminal 158 located on the same side of the device as the first terminal 21 and electrically connected to the second terminal 58 by a first electrical connection 160 formed between opposing sides of the device through region of insulating material 140 such that the first electrical connection 160 is insulated from the element of active material 23 [Col. 17, Lines 45-54, Figure 7].

With respect to claims 32 and 44, the claims are method counterpart of structure of the rejected claim 1 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 2, Inagaki discloses the first conductive interconnections and second conductive interconnections both comprise metal plating [Col. 20, Lines 10-17, Figure 7].

With respect to claim 36, the claim is a method counterpart of structure of the rejected claim 2 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 3, Inagaki discloses an electronic device 20 is a leaded device having a first lead 34 affixed to the first terminal 21 and a second lead 34 is affixed to the second terminal 22 [Col. 18, Lines 1-4, Figure 7].

With respect to claim 34, the claim is a method counterpart of structure of the rejected claim 3 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 5, Inagaki discloses the first electrical connection 160 comprises a plated through hole via [Col. 20, Lines 14-17; Col. 21, Lines 5-10, Figure 7].

Regarding claim 6, Inagaki discloses a leaded device 20 having a first lead 34 affixed to the first terminal and a second lead 34 affixed to third terminal 158 [Col. 18, Lines 1-4, Figure 7].

With respect to claim 37, the claim is a method counterpart of structure of the rejected claim 6 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 7, Inagaki discloses the device 20 is a surface mountable device and the first and third terminals (58, 158) provide SMT connections [Col. 17, Lines 40-50, Figure 8].

Regarding claim 8, Inagaki discloses a device 20 comprises a fourth terminal 158 located on the same side of the device as the second terminal 58 and electrically connected to the first terminal 58 by a second electrical connection 160 formed between opposing sides of the device 20 through the region of insulating material 140, 141 [Col. 17, Lines 45-54, Figure 7].

With respect to claim 38, the claim is a method counterpart of structure of the rejected claim 8 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 9, Inagaki discloses the second electrical connection 158 comprises a plated through hole via 160 [Col. 21, Lines 5-10, Figure 7].

With respect to claim 39, the claim is a method counterpart of structure of the rejected claim 9 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 12, Inagaki discloses the region of insulating material (30a, 30c, 38a, 38b, 40) comprises a printed circuit board 10 material having an aperture 30B defined therein in which the element of active material 23 is received [Col. 17, Lines 16-20, Figure 7].

With respect to claim 33, the claim is a method counterpart of structure of the rejected claim 12 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 17, Inagaki discloses the circuit board material is a laminate structure of glass bonded with a resin material [Col. 19, Lines 7-12].

With respect to claims 45 and 46, the claim are method counterpart of structure of the rejected claim 17 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 18, Inagaki discloses the first and second layers of insulating material (30a, 30c, 38a, 38b, 40) are provided as layers of resin [Col. 19, Lines 7-12].

With respect to claim 47, the claim is a method counterpart of structure of the rejected claim 18 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 20, Inagaki discloses the electronic device 20 is a leaded device and wherein leads 34 are fixed to the first 58 and third terminals 158 [Col. 18, Lines 1-4, Figure 7].

Regarding claim 21, Inagaki discloses at least one encapsulated electronic device 20 [Col. 17, Lines 17-20, Figure 7].

Regarding claim 28, Inagaki discloses the first, second, third and fourth terminals are suitably disposed to provide a symmetrical device [see Figure 7].

With respect to claim 55, the claim is a method counterpart of structure of the rejected claim 28 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 29, Inagaki discloses the terminals are metal plated [Col. 20, Lines 13-16].

Regarding claim 30, Inagaki discloses the metal plating is a combination of copper, nickel and/or gold [Col. 20, Lines 14-16] and [Col. 21, Lines 65-66].

Regarding claim 31, Inagaki discloses the plating comprises three separate metal plates of copper, nickel and gold [Col. 21, Lines 65-66, Figure 7].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 14, 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagaki in view of McGuire et al. [5884391].

Inagaki disclose the instant claimed invention discussed above except for the active material is a positive temperature coefficient material.

McGuire discloses an active material 20 is a positive temperature coefficient material [Col. 6, Lines 30-33, Figure 2].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a positive temperature coefficient material in the encapsulated electronic device as taught by McGuire to the device of Inagaki.

The motivation would have been for overcurrent protection of the circuit where the PTC is connected [Col. 1, Lines 36-38].

With respect to claim 42, the claim is a method counterpart of structure of the rejected claim 13 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Regarding claim 14, McGuire discloses the positive temperature coefficient material 20 is a polymeric material [Col. 6, Lines 32-33].

With respect to claim 43, the claim is a method counterpart of structure of the rejected claim 14 and method steps therefore are inherent for manufacturing encapsulated electronic device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joselito Baisa
Examiner
Art Unit 2832

jsb

ELWIN ENAD
SUPERVISORY PATENT EXAMINER
24 May 07